Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	186	clock adj2 enable with switch	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/21 12:03
L2	13	clock adj2 enable with switch with supply	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/21 12:07
L3	132	motherboard with laptop	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/21 12:07
L4	1	3 same ddr	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/21 12:07
L5	8	3 same slots	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/21 12:09
L6	28	3 and power.ab.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/21 12:09
S1	2	ddr adj2 termination adj2 array	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/20 12:42
S2	14	ddr adj2 array	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/17 14:49
S3	1436	termination adj2 resist$1rs	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/17 16:11
S4	2	S3 same power same memory near3 slot	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/17 16:11

S5	6	S3 same power same slot	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/17 16:11
S6	3612	$3connect$3 near5 terminat$3 with power	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/17 15:47
S7	155	S6 same mode	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/17 15:44
S8	12	S6 same low near3 mode	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/17 15:47
S9	1717	$3connect$3 near5 terminat$3 adj2 resist$4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/17 15:47
S10	104	disconnect$3 near5 terminat$3 adj2 resist$4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/17 15:54
S11	0	S10 same low near3 mode	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/17 15:53
S12	3	S9 same low near3 mode	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/17 15:53
S13	9	disconnect$3 near5 terminat$3 same low near3 mode	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/17 16:03
S14	2804	terminat$3 adj2 resist$1rs	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/17 16:11

S15	2	S14 same power same memory near3 slot	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/17 16:11
S16	8	S14 same power same slot	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/17 16:14
S17	11	S14 same voltage same slot	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/17 16:14
S20	144	terminat$3 with board with source	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/19 16:08
S21	3	S20 same slot	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/19 16:07
S22	16	terminat$3 with board with voltage adj2 source	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/19 16:17
S23	2255	control$4 same terminat$3 adj2 resist$4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/19 16:17
S24	960	control$4 with terminat$3 adj2 resist$4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/19 16:18
S25	27	control$4 with terminat$3 adj2 resist$4 with modules	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/19 16:24
S26	1	control$4 with terminat$3 adj2 resist$4 with slots	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/19 16:26

S27	556	control$4 with memory adj2 slot	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/19 16:27
S28	20	chipset with control$4 with memory adj2 slot	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/19 16:31
S29	0	chipset with coupl$3 with memory adj2 slot with terminat$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/19 16:30
S30	1	coupl$3 with memory adj2 slot with terminat$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/19 16:30
S31	6	chipset with control$4 with terminat$3 adj2 resist$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/19 16:32
S32	21	board with control$4 with terminat$3 adj2 resist$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/19 16:32
S33	2	ddr and termination adj2 array	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/20 12:42
S34	74	ddr and terminat$3 same motherboard	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/20 12:43
S35	12	ddr and terminat$3 same motherboard same slots	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/20 12:47
S36	13	ddr and terminat$3 same motherboard same slot	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/20 12:54

S37	146	power adj3 (mode or state) same $3connect$3 with terminat$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/20 13:17
S38	2	power adj3 (mode or state) same $3connect$3 with terminat$3 same motherboard	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/20 12:57
S39	5	power adj3 (mode or state) same $3connect$3 with terminat$3 same board	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/20 13:03
S40	16	power adj3 (mode or state) same $3connect$3 with terminat$3 adj3 resist$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/20 12:58
S41	3	power adj3 (mode or state) same $3connect$3 with terminat$3 same slot	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/20 13:04
S42	1	power adj3 (mode or state) same $3connect$3 with terminat$3 same slots	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/20 13:04
S43	7	S37 and ddr	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/20 13:05
S44	25	power adj3 (mode or state) same disconnect$3 with terminat$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/20 13:17